REMARKS

In view of the foregoing amendments and following remarks, reconsideration is requested. Claims 1-3 remain in this application, of which claim 1 is independent. No fee is due for claims for this amendment.

Rejections Under 35 U.S.C. §102

Claims 1-3, of which claim 1 is independent, were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,613,162 ("Kabenjian"). The rejection is respectfully traversed.

According to Kabenjian, during initiation, the CPU 100: writes a destination address, size of the transfer and other control data to the DMA controller 202; requests control of the memory bus 110; executes one or more read/write cycles addressed to the IDE device 156; initializes the DMA unit 200; writes to source, destination and count registers A; and writes go and direction data to the command register. See Kabenjian, col. 10, lines 5-61. After setting up the register set A 300 for a first DMA transfer, the CPU 100 either resets the first DMA channel for a second DMA transfer (col. 10, ll. 62-64), or uses a two-deep shadowing technique of "writing appropriate values to register set B of the first register block while the DMA unit is performing the previously initialized DMA transfer" (col. 11, ll. 3-6) or uses multiplexing to quickly switch between register set A or B. (col. 11, ll. 19-21).

The Final Office Action asserts that in Kabenjian, "[a]s a response of [winning] access on the bus the values in the parameter register is selected, as [disclosed] in col. 13, lines 15-17, "[t]hus, the values in the I/O parameter registers are selected to adapt the timing of the DMA transfers to the data transfer characteristics of the I/O device." Applicant disagrees. In Kabenjian, at Col. 13, lines 15-17, Kabenjian describes the initial static loading of registers performed by the system BIOS at initialization. The Final Office Action, on page 5, quotes Kabenjian as follows, with emphasis added by the Applicant: "In the preferred embodiment, the I/O device parameter registers are loaded by the system basic input/output system (BIOS) **during system initialization** because **at that time it will be known** which I/O devices are present and which DMA channels are dedicated to particular I/O resources. . .."

Therefore, the Office Action's factual finding that Kabenjian describes at Col. 13, lines 15-17 ""[a]s a response of [winning] access on the bus the values in the parameter register is selected" is not supported by substantial evidence. Accordingly, the rejection that relies on this erroneous finding should be withdrawn.

In contrast to Kabenjian, in claim 1, the DMA controller, not the CPU, *loads the stored parameters* (addressing, counters, pointers to buffer control units, etc.) that enable the data access between the port and the memory. Claim 1 recites (with emphasis added) "wherein the *direct memory access controller stores parameters* defining the direct memory access operations for each port, and wherein after a request is received from a port *the direct memory access controller loads the parameters for a direct memory access operation*, in response to the request from the port and independent of any instructions from a host central processing unit, to enable the port to access the memory and transfer data between the memory and the buffer associated with the port."

The Final Office Action asserts that the word "loads" in the claim is being interpreted as the parameters being selected. In Kabenjian, parameters are stored in registers by a CPU or BIOS, and then the register to be used by the DMA controller is selected. Nonetheless, to further clarify the claim, it has been amended to recited "loads registers used by the direct memory access controller with the parameters." Loading of registers with values distinguishes over Kabenjian's mere selection of DMA registers by a DMA controller. Accordingly, the rejection should be withdrawn for at least this reason.

The Final Office Action asserts that the claim "is also not detail in regards to when the CPU is not a part of a data transfer; in other words, is the CPU not a part during the initiation or during the transfer." Applicant disagrees. The claim plainly recites "after a request is received from a port the direct memory access controller loads the parameters for a direct memory access operation, in response to the request from the port and independent of any instructions from a host central processing unit." The CPU is not a part of loading the parameters by the DMA controller after the DMA controller receives a request from a port, as recited in the claim. To the extent the Office Action ignored this limitation, the rejection is erroneous and should be withdrawn for at least this reason.

Claim 1 also recites that the *buffer* is *located at and is dedicated to the port*. The Final Office Action asserts that this limitation is described by Kabenjian at col. 8, ll. 45-60. Applicant disagrees. The buffers 252-258 are clearly shown in Figs. 1-3 as being incorporated within Kabenjian's DMA unit 200 and described as "preferably" used for transfers with a particular I/O device. Therefore, the conclusion in the Office Action the Kabenjian's buffers 252-258 are located at and dedicated to the I/O ports in Kabenjian is not supported by substantial evidence. To the extent that the rejection relies upon this erroneous finding of fact, the rejection should be withdrawn.

In view of the foregoing amendments and remarks, the rejection of claims 1-3 in view of Kabenjian should be withdrawn.

New Claims

New claims 7-9 find support in and are similar to claims 1-3, but are directed to the direct memory access controller. Accordingly, claims 7-9 are patentable over the rejections of record for at least the same reasons as claims 1-3.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this reply, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If there is a fee occasioned by this response, including an extension fee, please charge said fee to **Deposit Account No. 50-0876.**

Accompanying this Reply is a Request for Continued Examination (RCE). Please charge the associated fee to **Deposit Account No. 50-0876.**

Respectfully submitted,

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